Application No.: 10/697,014

IBM Ref. No.: YOR920030204US1
CBLH Docket No.: 20140-00305-US1

AMENDMENTS TO THE CLAIMS

Please cancel claims 1-5 without prejudice to their reentry at some later date.

1 (Canceled).

2 (Canceled).

3 (Canceled).

4 (Canceled).

5 (Canceled).

6 (Original): An interconnect structure comprising an alloy of silver and an alloying element wherein the alloying element does not form a solid solution with the silver or an intermediate phase under 700°C and diffuses to the surface of the silver at temperature of 400°C or below, and is oxidizable to form an alloying element oxide having a conductivity of less than 10^{-5} reciprocal Ohm-cm; and a layer of the alloying element oxide of about 1 to about 10 nanometers on the alloy.

7 (Original): The interconnect structure of claim 6 where the alloying element is beryllium.

8 (Original): The interconnect structure of claim 7 wherein the amount of beryllium is about 0.2 to about 5% by weight.

9 (Currently amended): An electronic structure comprising

a dielectric layer having a substantially planar upper surface and having a pattern of recesses therein,

and an alloy ~~according to claim 1~~ being located in recesses wherein said alloy is an alloy of silver and an alloying element wherein the alloying element does not form a solid solution with the silver or an intermediate phase under 700°C and diffuses to the surface of the silver at a temperature of 400°C or below, and is oxidizable to form an alloying element oxide being of a conductivity of less than 10^{-5} reciprocal Ohm-cm; a layer of the alloying element oxide of about 1 to about 10 nanometers on the alloy.

10 (Original): The electronic structure of claim 9 wherein the alloy is present at the back end of the line (BEOL) of the structure.

11 (Original): The electronic structure of claim 9 wherein the alloying element is beryllium.

12 (Original): The electronic structure of claim 11 wherein the amount of beryllium is about 0.2 to about 5% by weight.

13 (Withdrawn): A method of fabricating an interconnect structure which comprises providing an alloy of silver and an alloying element wherein the alloying element does not form a solid solution with the silver or an intermediate phase under 700°C and diffuses to the surface of the silver at temperatures of 400°C or below;

and is oxidizable to form an alloying element oxide having a conductivity of less than 10^{-5} reciprocal Ohm-cm;

and selectively oxidizing the alloying element by annealing at temperature of about 250° to about 500°C in an oxidizing atmosphere containing an oxidizing agent having a partial pressure of about 10^{-8} to about 1 Torr forming a layer of alloying element oxide on the alloy.

14 (Withdrawn): The method of claim 13 wherein the oxidizing agent comprises oxygen or water vapor.

15 (Withdrawn): The method of claim 14 wherein the alloying element is beryllium.

16 (Withdrawn): The method of claim 15 wherein the amount of beryllium is about 0.2 to about 5% by weight.

17 (Withdrawn): A process for fabricating an interconnect structure on an electronic device which comprises:

forming a patterned resist layer on a substrate having insulating regions and conductive regions,

depositing an alloy according to claim 1;

and removing said pattern resist.

18 (Withdrawn): The process of claim 17 which further comprises selectively oxidizing the alloying element by

annealing at temperatures of about 250°C to about 500°C in an oxidizing atmosphere containing an oxidizing agent having a partial pressure of about 10^{-5} to about 1 Torr forming a layer of alloying element oxide on the alloy.

19 (Withdrawn): A process for fabricating an interconnect structure on an electronic device which comprises:

forming an insulating material on a substrate,

lithographically defining and forming recesses for lines and/or via in said insulating material in which interconnection conductor material will be deposited;

depositing an interconnection conductor material comprising an alloy according to claim 1; and

planarizing the resulting structure to provide electrical isolation of individual lines and/or vias.

20 (Withdrawn): The process of claim 19 which further comprises selectively oxidizing the alloying element by

annealing at temperatures of about 250°C to about 500°C in an oxidizing atmosphere containing an oxidizing agent having a partial pressure of about 10^{-8} to about 1 Torr forming a layer of alloying element oxide on the alloy.

21 (Withdrawn): A process for fabricating an interconnect structure on an electronic device which comprise:

depositing an insulating material on a substrate,

lithographically defining and forming lines and/or vias in which interconnection conductor material will be deposited,

forming a patterned resist layer on said insulating material depositing a conductor material comprising an alloy according to claim 1; and

removing the patterned resist.

22 (Withdrawn): The process of claim 21 which further comprises selectively oxidizing the alloying element by

annealing at temperatures of about 250°C to about 500°C in an oxidizing atmosphere containing an oxidizing agent having a partial pressure of about 10^{-8} to about 1 Torr forming a layer of alloying element oxide on the alloy.

23 (Withdrawn): A process of fabricating an interconnect structure on an electronic device which comprises:

depositing a blanket layer of conductor material on a substrate having insulating regions and conductive regions, wherein the conductor material comprises an alloy according to claim 1;

forming a patterned resist layer on said blanket layer,

removing said conductor material where not covered by said patterned resist, and

removing said patterned resist.

24 (Withdrawn): The process of claim 23 which further comprises selectively oxidizing the alloying element by annealing at temperatures of about 250°C to about 500°C in an oxidizing atmosphere containing an oxidizing agent having a partial pressure of about 10^{-8} to about 1 Torr forming a layer of alloying element oxide on the alloy.

25 (Withdrawn): A process for fabricating an interconnect structure on an electronic device which comprises:

forming an insulating material on a substrate,

lithographically defining and forming recesses for lines and/or via in said insulating material in which interconnection conductor material will be deposited;

depositing beryllium in said recesses;

depositing silver above said beryllium in said recesses;

annealing at temperatures of about 250°C to about 500°C.

26 (Withdrawn): The process of claim 25 wherein said insulating material comprises at least one member selected from the group consisting of silicon dioxide, phosphosilicate glass, boron doped PSG, tetraethylorthosilicate and a low-k dielectric material.

27 (Withdrawn): The process of claim 25 which further comprises providing a silver seed layer between said beryllium and silver.

28 (Withdrawn): The process of claim 25 which further comprises planarizing the resulting structure.

29 (Withdrawn): The process of claim 26 wherein said low-k dielectric material comprises at least one member selected from the group consisting of CVD porous carbon-doped oxide, non- porous carbon-doped oxide, porous spin-on organo silicates, non- porous spin-on organo silicates, porous spin-on organic polymers and non- porous spin-on organic polymers.

30 (New): The interconnect structure of claim 6, wherein said alloy consists essentially of silver and beryllium.

31 (New): The electronic structure of claim 9, wherein said alloy consists essentially of silver and beryllium.